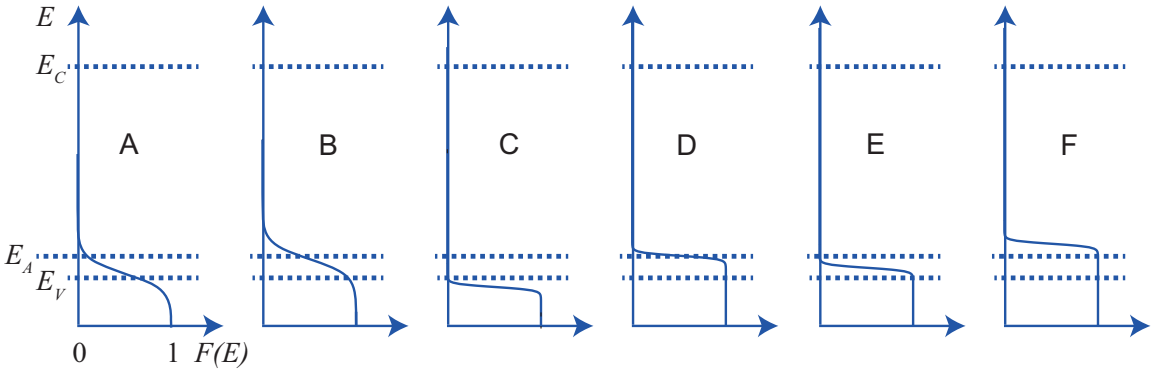
# Semiconductor Physics Problems 2019

*Page and figure numbers refer to Semiconductor Devices – Physics and Technology, 3rd edition, by SM Sze and M-K Lee*

1. The purest semiconductor crystals it is possible to fabricate have about 1 impurity per $10^{12}$ host atoms. Consider Si and answer the following questions:

   (a) What is the lowest possible concentration of impurities in a sample?

   (b) Given the result in (a), and assuming that the impurities act as dopants, is it possible for Si to exhibit intrinsic carrier concentrations at room temperature?




2. Figures A-F show the Fermi distribution in a semiconductor for different temperatures and doping conditions.

   (a) Which of the figures (A-F) best represents a p-type semiconductor where all dopants are ionized?

   (b) Which figure represents the highest $n$ (concentration of electrons in the conduction band)?

3. Consider two samples: an n-type sample of silicon with a uniform doping density $N_D = 10^{16}$ cm$^{-3}$ of arsenic, and a p-type silicon sample with $N_A = 10^{15}$ cm$^{-3}$ of boron. Determine the following:

   (a) For the n-type material: find the temperature at which half the impurity atoms are ionized. Assume that all mobile electrons originate from the dopant impurities.

   (b) For each material, find the temperature at which the intrinsic concentration $n_i$ exceeds the impurity density by a factor of 10.

   (c) Assume full ionization of impurities. Find the equilibrium minority-carrier concentrations in each material at 300 K.

   (d) Find the Fermi level, referred to the valence band edge $E_V$, in each material at 300 K. Find also the Fermi level if both types of impurities are present in the same sample (compensation doping)

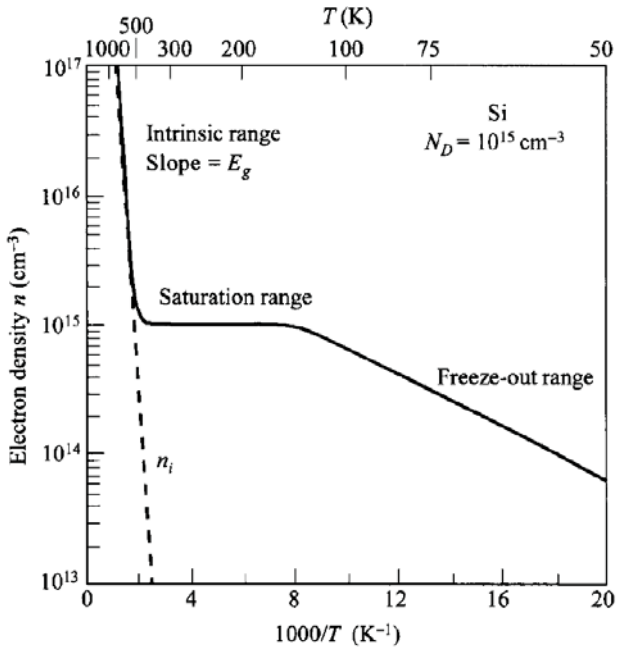



**Fig. 13** Electron density as a function of temperature for a Si sample with donor impurity concentration of $10^{15}$ cm$^{-3}$. (After Ref. 5.)

4. (a) Compare the figure above to figure 25 on page 39 in Sze (page 43 in 2nd edition). They essentially show the same kind of data. What is the difference between how data is plotted? Why do you think we prefer the representation above?

   (b) From the figure above, determine the ionization energy of the donor atoms used to dope the Si sample.

5. Consider the Fermi level for a boron-doped Si sample with an impurity concentration of $10^{16}$ cm$^{-3}$ at 300 K. Normally, at operational temperatures, we assume that all dopants are ionized (which allows us to compute for instance the Fermi level). However, all impurities cannot be ionized given the shape of the Fermi distribution.

   (a) Estimate the fraction of impurity atoms that are ionized. Assume full ionization, find $E_F$ and use this to evaluate the fraction of dopants that are ionized.

   (b) If you want an even better estime, you could make a small iteration.

   *Hint for (b): select a value for the concentration of ionized acceptors, which also gives you the concentration of holes. Use this to calculate $E_F$. Use this to evaluate the percentage of ionized acceptors from the Fermi distribution, which you can use to evaluate the $E_F$ again. If necessary, iterate a few times until consistent.*

6. For $p$ in a sample where $N_A > N_D$ we find $p$ as

$$p = \frac{1}{2}\left[N_A - N_D + \sqrt{(N_A - N_D)^2 + 4n_i^2}\right]$$

In what cases (see below) can we estimate that $p = N_A - N_D$? Use $n_i = 9.65 \cdot 10^9 \text{cm}^{-3}$ and $n_i = 2 \cdot 10^{13}$ cm$^{-3}$ for Si and Ge, respectively. All dopings in cm$^{-3}$.

(a) $N_A = 1 \cdot 10^{14}$ and $N_D = 1 \cdot 10^{12}$, Si sample

(b) $N_A = 1 \cdot 10^{14}$ and $N_D = 9 \cdot 10^{13}$, Si sample

(c) $N_A = 1 \cdot 10^{14}$ and $N_D = 1 \cdot 10^{12}$, Ge sample

(d) $N_A = 1 \cdot 10^{14}$ and $N_D = 9 \cdot 10^{13}$, Ge sample

7. Consider a compensated (contains both donor and acceptor impurity atoms in the same region) n-type Si sample at $T$ = 300 K, with a conductivity of $\sigma = 16(\Omega\text{cm})^{-1}$ and an acceptor doping concentration of $10^{17}$ cm$^{-3}$. Determine the donor concentration. Assume complete ionization and an electron mobility of $\mu_n = 1500$ cm$^2$/Vs. $n_i = 9.65 \cdot 10^9$ cm$^{-3}$.

8. **HAND-IN** Consider a Si sample doped with $1.0 \cdot 10^{14}$ cm$^{-3}$ of phosphorous atoms, $8.5 \cdot 10^{12}$ cm$^{-3}$ of arsenic atoms and $1.12 \cdot 10^{13}$ cm$^{-3}$ of boron atoms. Assume that all impurities are ionized and that the mobilities are $\mu_n = 1500$ cm$^2$/Vs, $\mu_p = 500$ cm$^2$/Vs, independent of impurity concentrations. $n_i = 9.65 \cdot 10^9$ cm$^{-3}$ in Si at 300 K.

(a) Find the resistivity of the sample.

(b) Find the Fermi level.

9. Consider two Si samples with high n-type dopings of $10^{17}$ cm$^{-3}$ and $10^{18}$ cm$^{-3}$, respectively. Calculate the Fermi level for the two samples. Compare the distances from the conduction band edge to $kT$. Are your results accurate? What was assumed when we derived the expressions for $n$ and $p$?

Modern devices often have regions with very high doping resulting in the semiconductor being degenerate, that is, the Fermi level is very close to or in a band.The semiconductor species also affects where the Fermi level end up given a certain doping density, since the effective mass enters in the effective density of states.

Consider n-type GaAs and find the Fermi level relative to the conduction band edge for $N_D = 10^{17}$ cm$^{-3}$ and $N_D = 10^{18}$ cm$^{-3}$ (same doping densities as for the Si just above). Is the GaAs degenerate?

10. Consider scattering in an n-type semiconductor sample by studying fig 2 on page 46 in Sze (p 50 in 2nd edition). Which of the following statements are true?

    (a) If doping level is increased a factor 10, conductivity is also increased a factor 10

    (b) At high $T$, lattice/phonon scattering dominates

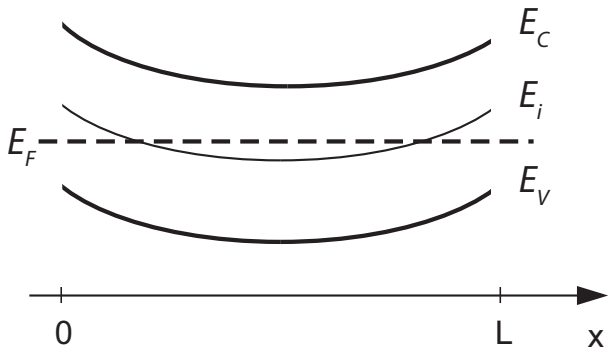
    (c) At room temperature, the scattering time due to lattice scattering is longer than that due to impurity scattering in lightly doped samples

    (d) If we could remove all impurities, the low $T$ scattering time would increase

11. Compute the average thermal velocity (speed) for holes in a Si sample at room temperature. Next assume that we apply a voltage of 1 mV over a 0.2 mm long section of the semiconductor. What is the drift velocity? Assume the hole mobility to be 400 $\text{cm}^2$/Vs.

12. Calculate the electron and hole concentration under steady-state illumination in n-type silicon with excess generation rate $G_L = 10^{16}$ $\text{cm}^{-3}\text{s}^{-1}$, $N_D = 10^{15}$ $\text{cm}^{-3}$ and $\tau_p = 10\mu\text{s}$.

13. Assume that an n-type semiconductor is uniformly illuminated, producing a uniform excess generation rate $G$. Show that in steady state the change in semiconductor conductivity is given by $\Delta\sigma = q(\mu_n + \mu_p)\tau_p G$.




14. The energy band diagram for a semiconductor is shown in the figure above. This may for instance represent the variation of potential along the radius of a n-type semiconductor nanowire with the Fermi level pinned close to the valence band edge at the nanowire surface by surface states.

    Sketch the general form of

    (a) $n$ and $p$ versus $x$,

    (b) the electrostatic potential $\Psi$ as a function of $x$,

    (c) the electric field as a function of $x$,

    (d) $J_n$ and $J_p$ versus $x$.

| region 1 | region 2 |
|---|---|
| $N_{D1} = 10^{17}$ cm$^{-3}$<br>$N_{A1} = 5{\cdot}10^{15}$ cm$^{-3}$ | $N_{A2} = 5{\cdot}10^{15}$ cm$^{-3}$ |

15. Consider a Si pn-junction with impurity concentrations as indicated in the figure above. Compute

    (a) The minority carrier concentration in region 1

    (b) The minority carrier concentration in region 2

    In order to compute the built-in potential $V_{bi}$,

    $$V_{bi} = \frac{kT}{q} \ln \frac{X_1 X_2}{n_i^2}$$

    which of the following suggestions for $X_1$ and $X_2$ would you use?

    (a) $X_1 = N_{D1}$ and $X_2 = N_{A2}$

    (b) $X_1 = N_{D1} - N_{A2}$ and $X_2 = N_{A2}$

    (c) $X_1 = N_{D1} - N_{A1}$ and $X_2 = N_{A2}$

    (d) $X_1 = N_{D1}$ and $X_2 = N_{A1}$

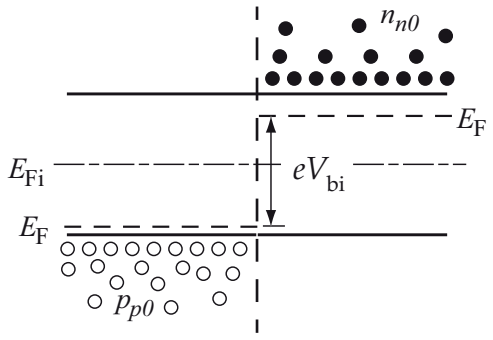
16. Consider an ideal silicon pn-junction with $N_A = 10^{17}$ cm$^{-3}$ and $N_D = 10^{15}$ cm$^{-3}$. Assume that all impurities are completely ionized.

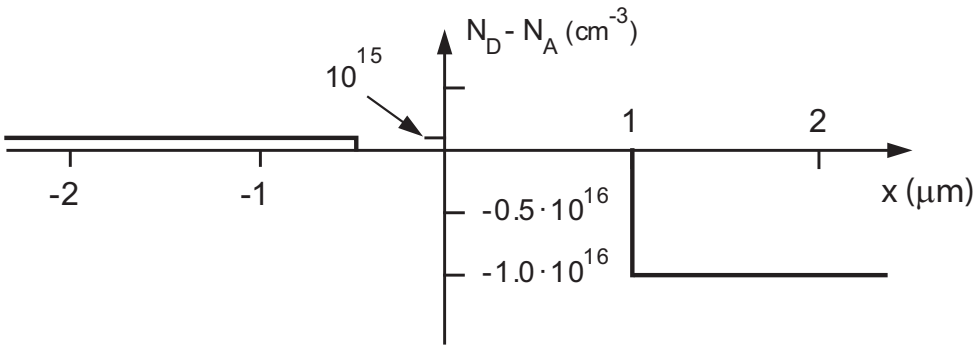
    (a) One approach to find the built-in voltage/potential is to consider the p- and n-part of the junction separately and find $V_{bi}$ as the difference between the Fermi-level $E_{Fn}$ on the n-side and the Fermi level $E_{Fp}$ on the p-side; $qV_{bi} = E_{Fn} - E_{Fp}$. Convince yourself that this gives an equation corresponding to equation 12 on page 85 in Sze (p. 91 in 2nd edition).

    (b) Calculate $V_{bi}$ at $T$ = 300, 350, 400, 450 and 500 K and plot $V_{bi}$ vs $T$.

    (c) Try to give a physical explanation for the trend observed in b). Hint: Maybe you can base your reasoning on the procedure in part a) or the figure below.

    (d) Find the depletion layer width and the maximum field at zero bias for $T$ = 300 K.





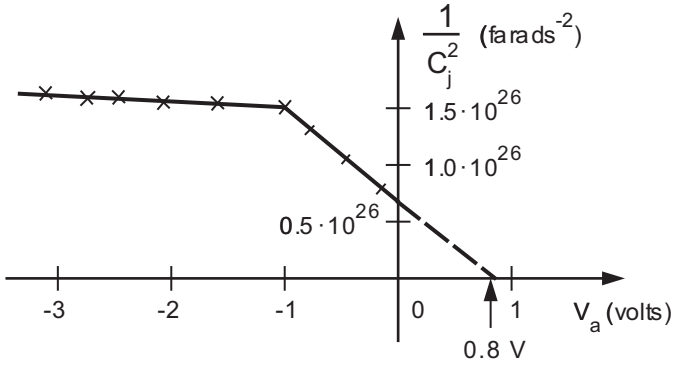

17. **HAND-IN** The figure shows the doping profile in a p-i-n junctioon; that is, a pn-junction with a very lightly doped or nearly intrisic region in the center. To clarify the figure: the doping density is $10^{15}$ cm$^{-3}$ on the n-side and $10^{16}$ cm$^{-3}$ on the p-side.

    (a) Sketch the charge density, the built-in electric field and the potential for a silicon pin junction with the doping profile shown in the figure above.

    (b) Calculate $V_{bi}$ and the length of each depletion region at thermal equilibrium.

    (c) Calculate the magnitude of the maximum field in the pin junction. Compare it to the maximum field in a pn junction that contains no lightly doped intermediate region, but has the same dopant concentrations as in part (a) in the other regions.

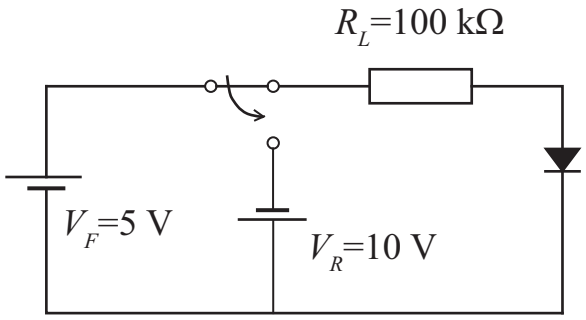
    (d) Make a sketch indicating how the built-in electrical field in the pin junction changes when a reverse bias is applied.




18. **HAND-IN** The depletion layer capacitance $C_D$ (denoted $C_j$ in the plot above) of a Si pn junction diode with area $10^{-5}$ cm$^2$ is measured. A plot of $(1/C_D^2)$ vs. the applied voltage $V_a$ is shown in the figure above. Note that the capacitance is not given as a capacitance per unit area, but as the capacitance for a device of a specific size.

    (a) If the diode is considered as a one-sided step junction, where the p-side is heavily doped (that is, a p$^+$n junction), find the doping level on the n-side.

    (b) Calculate the location of the point (distance from the actual junction) on the n-side at which the dopant density changes, and include this point in your sketch. How does the dopant density change at this point – does it increase or decrease compared to the value you found in a)? Make a qualitative sketch showing the doping density on the n-side of the p$^+$n junction.




19. **HAND-IN** In an ideal p$^+$n silicon diode with $N_D = 10^{15}$ cm$^{-3}$ and $N_A = 10^{18}$ cm$^{-3}$ the hole lifetime is 1 $\mu$s and their mobility 450 cm$^2$/Vs. The area of the diode is 0.1 mm$^2$. ("Ideal" implies that effects within the space-charge region are negligible and that minority carriers flow only by diffusion mechanisms in the charge neutral regions.)

    (a) Determine the current in the diode when reverse biased. This is accompliced by flipping the switch in the figure above (as indicated).

    (b) Estimate the stored minority carrier charge when the diode is forward biased in the circuit above. *Hint: what is the voltage drop over the diode in this case?*

    (c) Turning the switch will reverse bias the diode. Determine the change in fix charge in the depletion region on the n side when the diode is switched from forward to reverse bias. *Note: this problem concerns fix charge as opposed to carrier charge.*

20. Consider an ideal, long-base, silicon abrupt pn-junction diode with uniform cross section and constant doping on either side of the junction. The diode is made from 1 Ω-cm p-type and 0.2 Ω-cm n-type materials in which the minority-carrier lifetimes are $\tau_n = 10^{-6}$ s and $\tau_p = 10^{-8}$ s, respectively. You may find figure 7 on page 51 of Sze (p 55 in 2nd edition) and fig 3 on page 47 (p 51) useful.

    (a) What is the value of the built-in voltage (built-in potential)?

    (b) Calculate the density of the minority carriers at the edge of the space-charge region when the applied voltage is 0,589 V (which is $23kT/q$).

    (c) Sketch the majority- and minority-carrier currents as functions of distance from the junction on both sides of the junction, under the applied bias voltage of part b.

    (d) Calculate the location(s) of the plane or planes at which the minority-carrier and majority-carrier currents are equal in magnitude for the applied bias of part b.

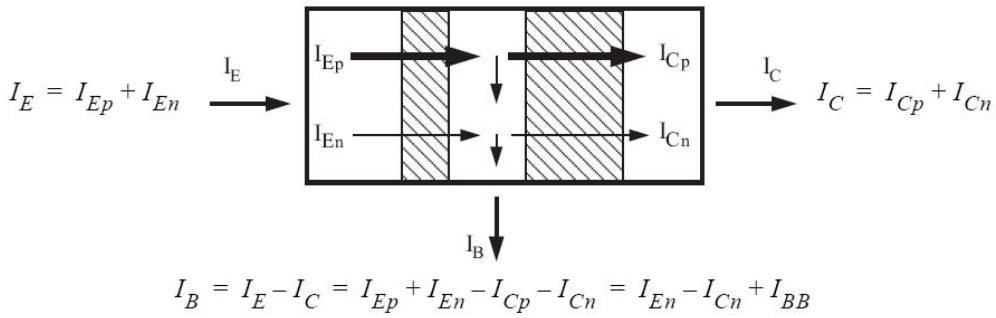
21. (a) For forward voltages between 0 and 0.6 V, plot (on a logarithmic scale) the diffusion current in a Si $p^+n$-junction. In the same plot, include also the recombination current (page 106, p 110 in 2nd edition). You may assume $N_D = 10^{15}$ cm$^{-3}$, $\mu_p$ = 500 cm$^2$/Vs and $D_p$= 10 cm$^2$/s and a life-time $\tau_p = \tau_n = 1\mu$s. For the purpose of calculating the built-in potential you can use for instance $N_A = 10^{17}$ cm$^{-3}$.

    (b) Finally, plot the sum of the two current contributions, also in the same plot. Try to identify regions with ideality factor 1 or 2 (see page 106, p 112 in 2nd edition) for definition of ideality factor)

22. A Si npn transistor has impurity concentrations of $5 \cdot 10^{18}$ cm$^{-3}$, $2 \cdot 10^{17}$ cm$^{-3}$ and $10^{16}$ cm$^{-3}$ in the emitter, base and collector, respectively. The p-type base width is 1.0 $\mu$m, and the device cross-sectional area is 0.2 mm$^2$. When the emitter-base junction is forward biased to 0.5 V and the base-collector junction is reverse biased to 5 V, calculate

    (a) the neutral base width and

    (b) the minority carrier concentration in the base at the edge of the emitter-base junction depletion region.




23. **HAND-IN** The figure above depicts a pnp bipolar transistor and all the currents which we consider in it.

    (a) Draw an equivalent figure, still for a pnp-transistor, where you instead of currents draw electron and hole flows.

    (b) Draw an equivalent figure for a npn transistor, where you draw currents. Label the currents in a way appropriate to the npn-transistor.

    Make nice big figures, so that everything is clearly visible.

24. **HAND-IN** Consider Eq. 14 on p. 130 in Sze (2nd edition; see Eq. (14) p. 138) for the distribution of minority carriers in the base of an pnp bipolar transistor in the active mode (EB junction forward biased and BC junction reverse biased). The equation can be reorganized to read:

$$p_n(x) - p_{n0} = (p_n(0) - p_{n0})\frac{\sinh(\frac{W-x}{L_p})}{\sinh(\frac{W}{L_p})} + (p_n(W) - p_{n0})\frac{\sinh(\frac{x}{L_p})}{\sinh(\frac{W}{L_p})}$$

where $x = 0$ and $x = W$ are the edges of the neutral base.

(a) For a Si pnp-transistor, plot $p_n(x)/p_{n0}$ as a function of $x$ for different values of $W$. In your plot, include the following neutral base widths $W$:

$W/Lp$ = 5, 2, 1, 0.5, 0.1 and 0.01.

All six graphs should be in the same plot. Make sure it is indicated which graph represents which base length. You can assume $V_{EB} = 0.5$ V, $V_{CB} = -1$ V, $N_B = 10^{16}$ cm$^{-3}$ and $L_p = 10^{-4}$ cm (the minority carrier diffusion length in the base).

(b) Using the plots in a), evaluate the ratio $I_{Cp}/I_{Ep}$ for the different base widths $W$. *Hint: the currents can be obtained by estimating the gradients of the minority carrier distributions.*

Make a graph where you plot the ratios $I_{Cp}/I_{Ep}$ for different $W$ vs $W$. Since $W$ varies over several orders of magnitude, you need to use a logarithmic scale on the $W$-axis. Verify your results by comparing your ratios to the theoretical ratio $I_{Cp}/I_{Ep} = 1/\cosh(W/L_p)$. Plot the theoretical values in the same plot as your calculated values.

(c) Write a short text (150 words is sufficient) describing how your plots are significant to our discussion of bipolar transistors.

25. **HAND-IN** Consider a Si ***npn*** transistor. The area of the device is $1.2 \cdot 10^{-4}$ cm$^2$. In absence of applied bias, the neutral base width is $4 \cdot 10^{-4}$ cm. For the transistor we further have:

| | | |
|---|---|---|
| $N_E = 3.9 \cdot 10^{17}$ cm$^{-3}$ | $N_B = 1.6 \cdot 10^{16}$ cm$^{-3}$ | $N_C = 2 \cdot 10^{14}$ cm$^{-3}$ |
| $L_E = 22.8 \cdot 10^{-4}$ cm | $L_B = 46.9 \cdot 10^{-4}$ cm | $L_C = 39.5 \cdot 10^{-4}$ cm |
| $D_E = 5.18$ cm$^2$/s | $D_B = 22$ cm$^2$/s | $D_C = 15.6$ cm$^2$/s |

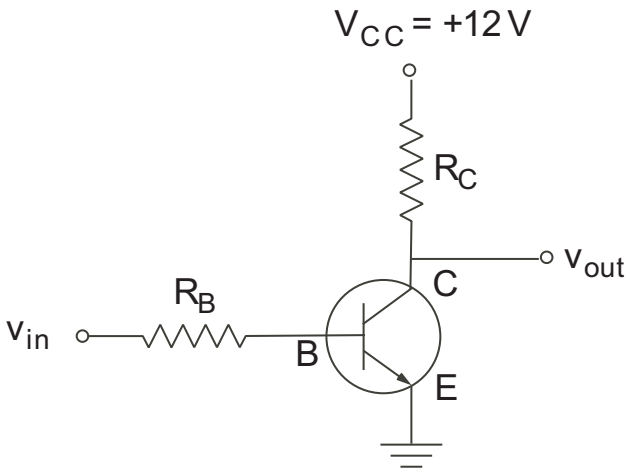
(a) For a forward bias of $V_{EB} = 0.6$ V on the emitter-base junction, calculate $I_{En}$ and $I_{Ep}$ (it is OK to use the expressions for current for short bases, that is, when $W/L_n < 1$). Also calculate the emitter efficiency $\gamma$ . You don't need to care about the change in $W$ due to biasing.

(b) What is the emitter efficiency if the emitter is doped to the same level as the base, that is, $N_E = N_B = 1.6 \cdot 10^{16}$ cm$^{-3}$?

26. For the transistor of problem 25, consider the emitter-base junction open-circuited and the base-collector junction reverse biased by -1 V. Find $V_{EB}$ and $I_{CBO}$ (that is the current in the base-collector junction when the emitter current is zero).

    The neutral base width in the absence of applied biases is stated in problem 25. Here, there is a reverse bias applied to the base-collector junction. Since the collector is lightly doped the depletion region at the base-collector junction will expand mainly into the collector, and thus the base width will not be significantly reduced. You can use the value of problem 25 as the base width $W$.

27. Consider the lower image on p 72 of the notes. It shows band diagrams for a pnp-transistor in the four modes of operation. Draw the equivalent images for a npn transistor. By equivalent we mean that the axes stay the same, for instance that a positive $V_{EB}$ means $V_E > V_B$. This will forward bias the EB-junction in a pnp-transistor, but what is the effect in a npn-transistor?




28. The transistor in the circuit shown in the figure above has a common-emitter current gain $\beta = 100$.

    The resistors in the circuit are $R_C = 1$ k$\Omega$ and $R_B = 20$ k$\Omega$. Assume $V_{EB} = 0.6$ V for the forward biased EB junction.

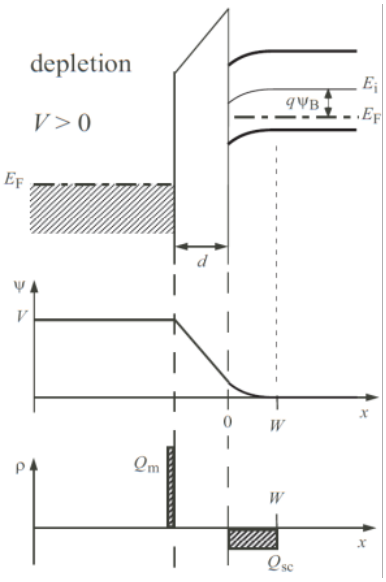
    Determine $v_{out}$ for $v_{in} = 1$ V and 2 V.

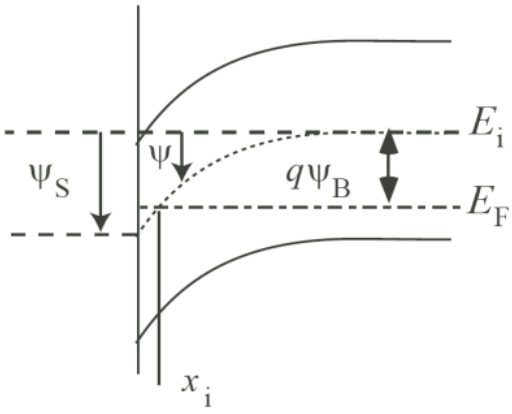
29. For an ideal MOS with a n-type semiconductor under inversion, plot

    (a) the space charge distribution

    (b) the electric field

    (c) the potential




30. We want to find the threshold voltage $V_T$ for inversion in a p-type Si MOS in terms of material constants, such as dielectric constants, and in terms of parameters that we control, such as doping level. The voltage $V_T$ is split between the oxide and the semiconductor, so that $V_T = \Psi_S + V_0$.

    The band bending (in inversion) is primarily given by the depleted region in the semiconductor. Here, we have a space charge density $\rho = -qN_A$ for $0 \leq x \leq W$ (see figure). From that we find the potential

    $$\Psi(x) = \frac{qN_A}{2\varepsilon_s}(x - W)^2 = \Psi_s(1 - \frac{x}{W})^2$$

    where $\Psi_s = \frac{qN_A}{2\varepsilon_s}W^2$

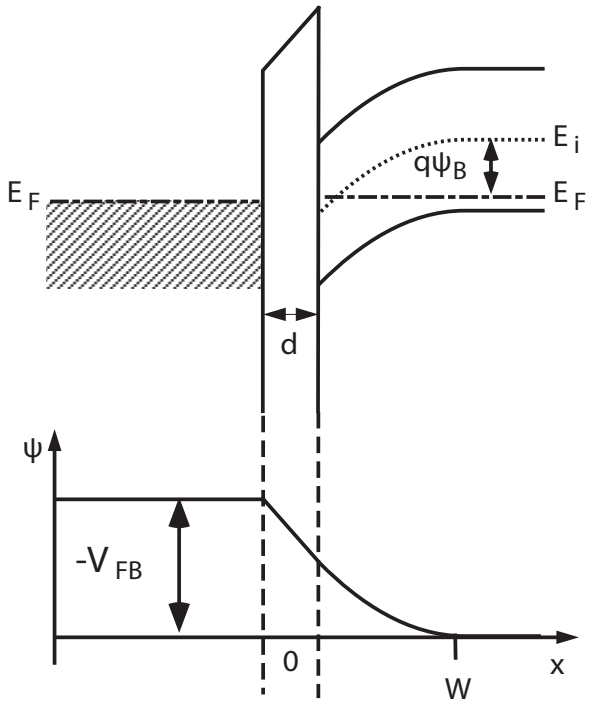
    (a) Deep in the p-type semiconductor $p_{p0} = N_A$. Start from $p = n_i e^{(E_i - E_F)/kT}$ and show that $\Psi_B = (kT/q)\ln(N_A/n_i)$

    (b) In strong inversion the electron concentration at the surface $n_s \geq N_A$. Starting from $n_s = n_i e^{(E_F - E_{is})/kT}$, where $E_{is}$ is the intrinsic Fermi level at the surface, show that $E_F - E_{is} = \Psi_B$ when $n_s = N_A$. The potential at the surface thus has to be $\Psi_S = 2\Psi_B$ for inversion.

    (c) Now consider the voltage drop $V_o$ over the oxide. From electrostatics, we found that $V_o = d \cdot \frac{Q_m}{\varepsilon_{ox}} = d \cdot \frac{|Q_s|}{\varepsilon_{ox}}$. At the onset of strong inversion, $|Q_s|$ can be approximated by $|Q_{sc}|$ where $Q_{sc}$ is the charge from the depleted acceptors. In inversion, $Q_{sc} = -qN_A W_m$.

    Show that the depletion region width $W$ can be written in terms of the surface potential as $W = \sqrt{\frac{2\varepsilon_s \Psi_s}{qN_A}}$ (see beginning of problem) and that, consequently, in inversion, $W_m = \sqrt{\frac{2\varepsilon_s 2\Psi_B}{qN_A}}$.

    (d) Now we put our results together. Show that the threshold voltage $V_T = \Psi_s(\text{inv}) + V_o = \frac{2kT}{q}\ln\frac{N_A}{n_i} + \sqrt{\frac{4\varepsilon_s N_A d^2}{\varepsilon_{ox}^2} kT \ln\frac{N_A}{n_i}}$




31. **HAND-IN** For the Si MOS structure above, the work function in the metal is smaller than that of the semiconductor by 1V (we disregard any oxide charges). The potential in the metal relative to in the semiconductor, $|V_{FB}|$, is the sum of a potential drop over the oxide and a potential drop over the depleted region of the semiconductor. Consider the semiconductor to be grounded. The oxide thickness $d = 10$ nm, the oxide permittivity is $\varepsilon_{ox} = 3.9\varepsilon_0$ and $N_A = 10^{17}\text{cm}^{-3}$.

    (a) What is the value of the surface potential?

    (b) What is the electric field in the oxide?

    (c) What are the values of electron and hole concentrations at the surface of the semiconductor?

32. Consider a MOS device on a p-type substrate ($N_A = 10^{17}\text{cm}^{-3}$) with 20 nm of gate oxide. The gate is made of polycrystalline $n^+$-Si. When used as a gate electrode, the $n^+$-Si is very heavily doped and essentially the Fermi level coincides with the conduction band edge.

    (a) Find the work function difference between the polycrystalline Si gate and the p-type Si semiconductor.

    (b) Find $V_T$.

    (c) Make a sketch of the $C - V$ curve measured at high frequencies. In your sketch, label (roughly) $V_T$ and $V_{FB}$.

    (d) Calculate $C_{min}$ and $C_{max}$ (still for high frequency).

33. A Si MOSFET has the following dimensions and characteristic parameters: $L = 1$ $\mu$m, $Z = 1$ $\mu$m, $N_A = 10^{17}$ cm$^{-3}$, $\mu_n = 800$ cm$^2$/Vs and the Si oxide thickness is 20 nm. The semiconductor work function is 3.8 V and the gate work function is 4 V.

    (a) Sketch the band diagram at thermal equilibrium and at threshold condition $\Psi_s = 2\Psi_B$. What is the threshold voltage?

    (b) Calculate the drain current for $V_G = 2.2$ V and $V_D = 0.3$ V.

    (c) Calculate the drain current for $V_G = 2.5$ V and $V_D = 0.3$ V.

34. A n-channel MOSFET is made on p-type silicon with $N_A = 4 \cdot 10^{15}$ cm$^{-3}$.

    (a) Determine the threshold voltage under the assumption that the oxide (rel. dielectric constant 3.9) is free of charge and that difference in work functions may be neglected. The gate oxide is 100 nm thick.

    (b) Sketch the drain current vs the gate voltage for the MOSFET of part a) if drain and gate are connected and source and substrate are grounded. Can the threshold voltage be determined from the characteristic?

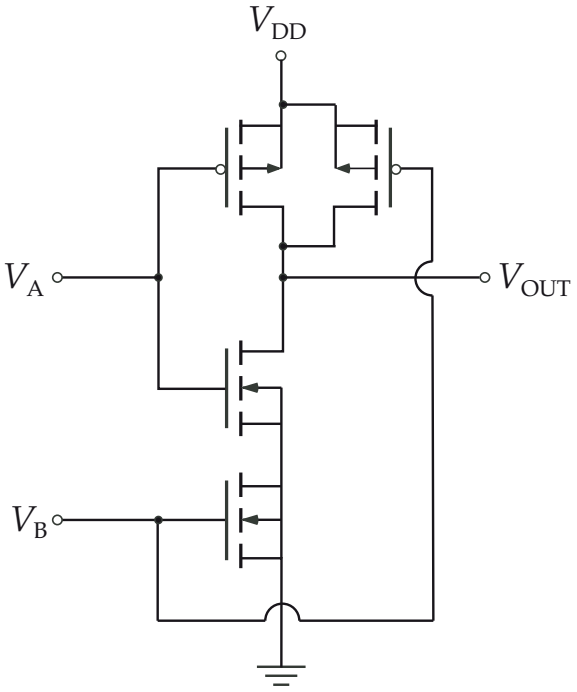
35. Threshold voltage control is an important concept. In devices such as CMOS (Complimentary MOS – one PMOS and one NMOS acting together as for instance an inverter) and generally in circuits, we may want to tailor the threshold voltage. There are several approaches to this.

    Consider a N-MOS with gate and semiconductor parameters as in problem 32.

    (a) Is the N-MOS conducting at $V_G = 0$?

    (b) Find the change in doping necessary to change $V_T$ by $-0.5$ V. Here, we assume that the doping is changed to a large depth in the semiconductor, not only just below the oxide.

    (c) Find the change in oxide thickness needed to accomplish the same shift of $V_T$ as in b)




| $V_A$ | $V_B$ | $V_{OUT}$ |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

36. **W**e have discussed the CMOS inverter, or logical NOT gate, in class, but one can also build other logical gates using MOSFETs.

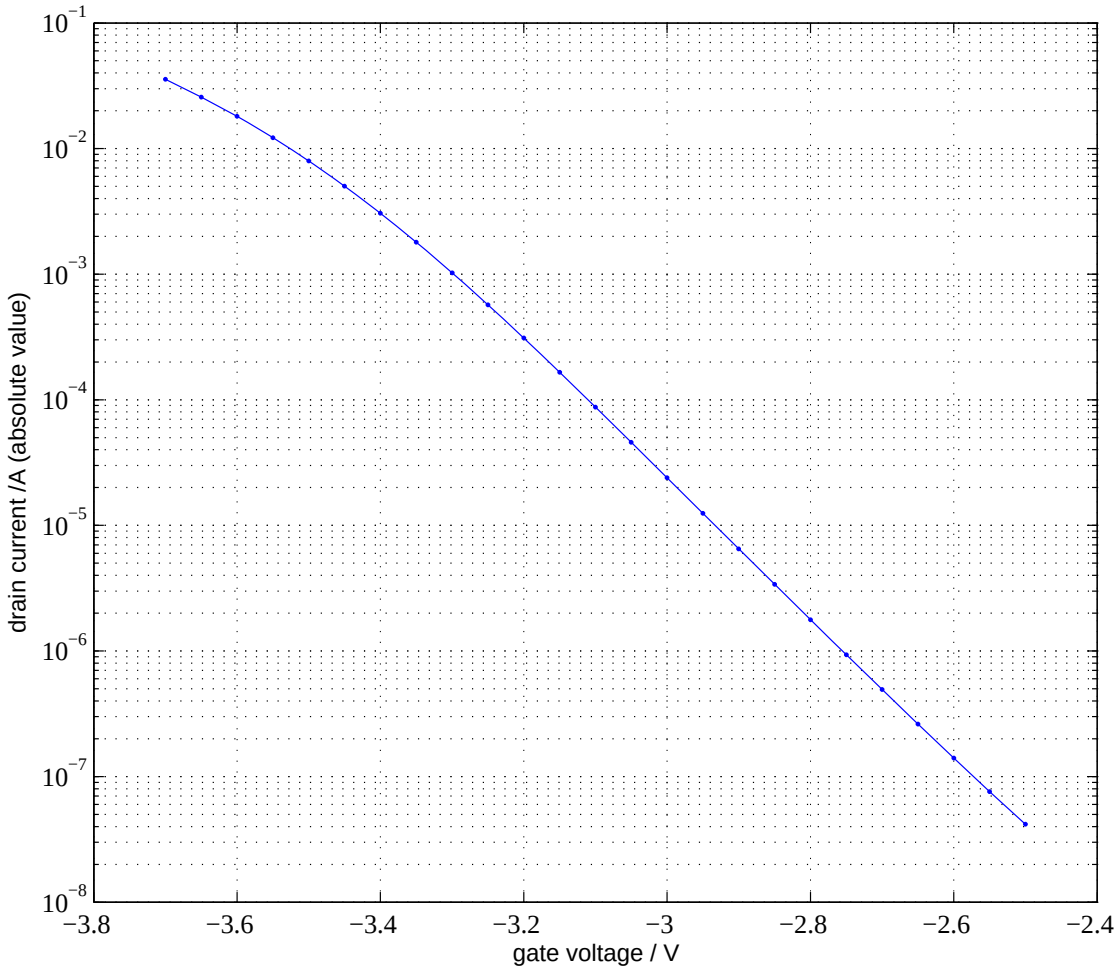
    In the figure, the two lower transistors are NMOS and the two upper are PMOS. This circuit takes two input voltages, $V_A$ and $V_B$, and gives one output $V_{OUT}$. $V_{DD}$ is some high voltage comparable to $V_A$ and $V_B$. We assume that these voltages are greater than the threshold voltages of the transistors.

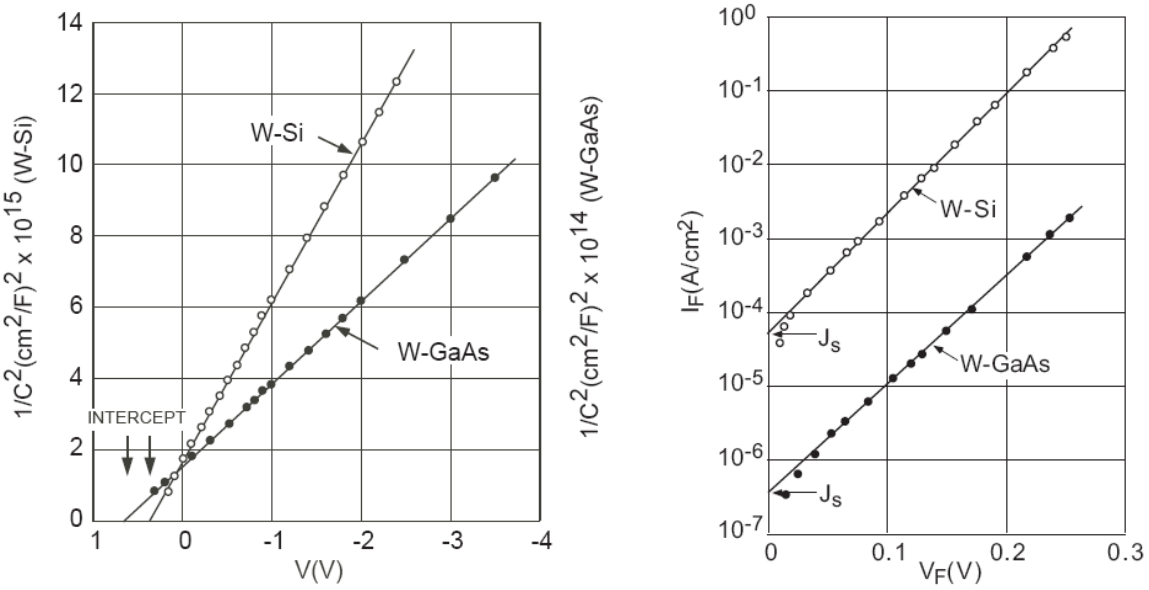
    In describing a logical gate, a low voltage is denoted 0 and a high voltage 1. Make a truth table as indicated in the figure. For each setting, figure out if the output is high (1) or low (0). What logical operation does this circuit perform?

37. **HAND-IN** A MOSFET has a threshold voltage of $V_T = 0.5$ V, a subthreshold swing of 100 mV/decade, and a drain current of 0.1 mA at $V_T$.

    (a) What is the subthreshold leakage current at $V_G$ = 0V? (Hint: think about what the subthreshold swing really means.)

    (b) In the MOSFET lab, you measured drain current as a function of gate and drain voltage. The figure shows the drain current at a fixed $V_D > V_{Dsat}$) for varying $V_G$ for one of the devices in the lab. Was it the NMOS or the PMOS and what is the subthreshold swing?






38. **HAND-IN**

    (a) Find the barrier height and the donor concentration of the W- GaAs Schottky barrier shown in the capacitance plot above left. *Note that the plot shows two different data-sets - make sure you read values of the correct $y$-axis.*

    (b) Compare the barrier height with that obtained from the saturation current density shown in the current plot above right, assuming that $A^* = 4$ A/(cm-K)$^2$.

39. Compare a Schottky diode fabricated on n-GaAs and a p+n diode (also GaAs). The reverse saturation currents are $I_s = 5 \cdot 10^{-9}$ A and $I_0 = 10^{-13}$ A for the Schottky diode and the pn-junction, respectively. What voltage is required for each device in order to have 0.5 mA pass through it?

40. This problem concerns the discussion in the Sze e-book (which is linked from the course homepage). The relevant pages are 139-144. See also notes.

    (a) In figure 6 on page 143 we notice that $c_2 = 0.27$ is relevant for Si. This number thus tells us something about the nature of the population of surface states in Si. Assuming an interface layer with thickness $\delta = 5$Å and permittivity $\varepsilon_i = \varepsilon_0$ and a semiconductor doping of $N_D = 10^{18}$cm$^{-3}$, calculate the density of interface states $D_{it}$. (check your answer on page 142).

    (b) If the Fermi level does not coincide with the neutral level, there will be a net charge at the interface. By how much can the Fermi level deviate from the neutral level in order for the interface charge $Q_{ss}$ to not become greater than the semiconductor charge $Q_{sc}$ (from ionized dopants)? Here you will have to obtain a value for $V_{bi}(\Psi_{bi})$ at some point. Either you can just assume some reasonable value, or use fig. 5 on page 140 in the book. $\Psi_{bi} = E_g - q\phi_n - q\phi_0$, if we make the approximation that $E_F$ coincides with $\phi_0$ (not completely true, but not far from the truth either, it will do as an estimate). $\phi_0$ is calculated at the bottom of p. 142.