Laboratory Exercise: Short-Channel MOSFETs

Semiconductor Physics (FFF021) 2016

Lab meeting point: k-space, Solid State Physics

Preparation before the lab

You should read the following pages in *Semiconductor devices: Physics and technology*, 3rd ed., Sze:

Advanced MOSFET and related devices: p. 196 – 205

Challenges for nanoelectronics: p. 538 - 543

Introduction

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{dD}, x_{dS}) of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects (SCE) arise.

The purpose of the lab is to gain some insight into issues that arise as the MOSFET gate length *L*, that is the distance between the source and drain regions, is decreased. This will result in *drain-induced barrier lowering*, which limits the gate control over the channel and may lead to leakage during off-conditions.

There are a few techniques to mitigate the SCE effect in MOSFETS, e.g.:

- Silicon on Insulator (SOI)-MOSFET

- Increase k-value of the gate oxide

- Multigate (3D) structures (FinFET, Nanowires)

The lab is based on simulations in the Silvaco software, which you have already used in two previous labs. Initially you will remind yourself of some properties of MOSFETs studied in the MOSFET lab, next you will study how these properties change as gate length is decreased. The property we are particularly interested in is the band edges below the gate, as they show the gate control over the inversion channel. Finally, if you have time, you will study one of the designs to reduce short-channel effects.

Start the simulation tool Silvaco Deckbuild (shortcut on the desktop). For the software license, the computer must be connected to the license server via LU Web-logon.

Part 1: Long-channel MOSFET

Load *ShortChannelMOSFET2016.in* located in *c:\SilvacoWork\Short-channel MOSFET*. Run the simulation by clicking the green arrow.

In this simulation, we will study a MOSFET structure under a number of different bias conditions:

1. $V_G = 0$ V. $V_D = 0$ V.
2. $V_G = 0$ V. $V_D = -2.5$ V.
3. $V_G = 0$ V. $V_D = -5$ V.
4. Two transfer sweeps – $V_D = -2.5$ V and -5 V. V_G from 0 to -2 V.
5. Two output sweeps – $V_G = -0.6$ V and -1.5 V. V_D from 0 to -5 V.

- Bias conditions 1,2,3 will be plotted in the same 2D plot. Start by investigating this plot.
- Right-click – display – select contours and electrodes, deselect edges. Study the doping profile. How long is the channel? In the display window, click Define Contours and select Conduction Band Energy. Study the depletion regions.
- Define a horizontal cutline and study the band diagram. Is this a pMOS or nMOS? In which operation mode is the transistor? Is the barrier height affected by the drain bias?
- Define a vertical cutline and study the band diagram. Is the gate controlling the charge in the entire channel? Where would the current punch through first if we increased the drain voltage?

- Study the output sweeps (plot I_D vs V_D). Can you see any short-channel effects?
- Study the transfer sweeps (plot I_D vs V_G). Measure the approximate threshold voltage using the ruler tool.
- Discuss – why is it beneficial to scale down MOSFETs? Which device dimensions are scaled and how are the device characteristics affected?

Part 2: Short-channel MOSFET

Set the parameter scaleFactor to 10. Check in the code which parameters are affected. Run the simulation by clicking the green arrow.

- Right-click – display – select contours and electrodes, deselect edges. Study the doping profile. How long is the channel now? In the display window, click Define Contours and select Conduction Band Energy. Study the depletion regions and compare to the long-channel device.
- Define a horizontal cutline and study the band diagram. Is the barrier height affected by the drain bias now? What is this effect called?
- Define a vertical cutline and study the band diagram and hole concentration. Is the gate controlling the charge in the channel?

- Study the output sweeps (plot I_D vs V_D). Can you see any short-channel effects? Relate this to the band diagram.
- Study the transfer sweeps (plot I_D vs V_G). Measure the approximate threshold voltage. How does it compare to the long-channel device? What is this effect called?

- How thick is the gate oxide? Can that be a problem? How can it be mitigated?

Part 3: FinFET (if you have time)

In a FinFET, the channel is a very thin vertical fin structure. The gate is wrapped around the fin and controls the channel from three directions. This structure needs to be simulated in three dimensions, so the number of elements required in the simulation, and thus the computing time, increases radically.

To properly simulate the characteristics of this transistor, we would need to account both for quantum confinement effects in the thin channel and the ballistic transport of charge carriers through the channel. The latter starts to become important when the channel length approaches the carrier mean free path and some carriers move through the channel without scattering. However, as we are mostly interested in studying the band structure we may use the same physics that we used in the previous examples and are more familiar with.

This simulation requires a lot more computing power than the previous ones, so we will load saved data from a simulation computed on a more powerful workstation. $V_G = 0V$ and $V_d = 0, 0.1, 0.2, 0.3$ V.

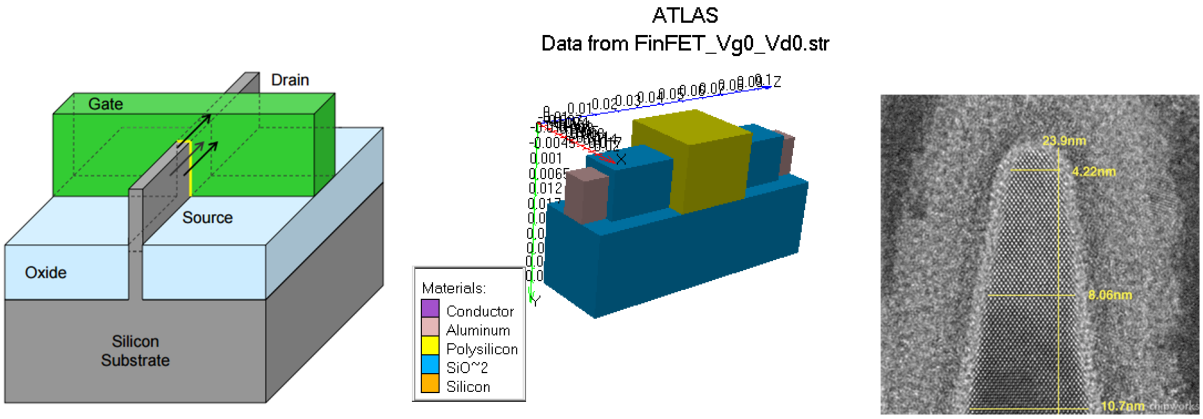

Figure 1. Left: Intel FinFET. Source: Intel.com. Center: The FinFET we study in this lab. Note that the channel is completely insulated from the silicon substrate in the simulated transistor.Right:TEM cross-section showing the top of the fin in an Intel FinFET. Source: Electronicsweekly.com.

- Start TonyPlot3D. Load the file *FinFET_Vg0_Vd0.str* located in *c:\SilvacoWork\Short-channel MOSFET*. Study the structure of the transistor. Define a cut plane in the center of the channel, parallel to the fin (Pan=90, Pitch=0, Elevation=0).
- Start TonyPlot (not 3d). Load all the FinFET cut plane files *FinFET_Vg0_Vd0_cutplane.str, FinFET_Vg0_Vd01_cutplane.str* (…). into an overlay plot. Make sure you understand what you are looking at. How long is the channel? Use the cutline tool to study the band structure and electron concentration both in the horizontal and vertical directions. Is this a pMOS or nMOS? What can we say about the gate control?
- Open *FinFET.in* and study the code. What gate oxide is used? Can we improve that? What other parameters can we change to reduce the short-channel effects?