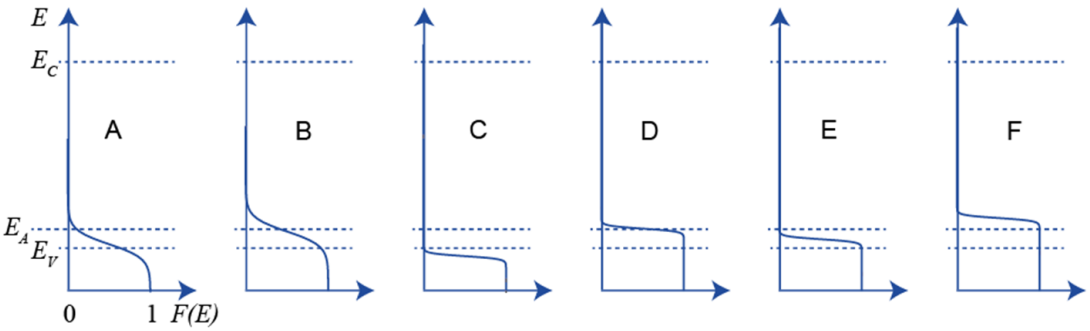
Semiconductor Physics fall 2014– problems



1. a) Which of the figures (A-F) best represents a p-type extrinsic semiconductor where all dopants are ionized?

   b) Which figure represents the highest *n* (concentration of electrons in the conduction band)?

2. An n-type sample of silicon has a uniform density $N_D = 10^{16}$ atoms cm^{-3} of arsenic, and a p-type silicon sample has $N_A = 10^{15}$ atoms cm^{-3} of boron. Determine the following:

a) Consider the n-type material. Find the temperature at which half the impurity atoms are ionized. Assume that all mobile electrons come from the dopant impurities. Use the Fermi distribution (eq. 16 on page 17 and also in the notes) – not the distributions functions on page 22 of Sze.
b) Find the temperature at which the intrinsic concentration n_i exceeds the impurity density by a factor of 10 (for each material).
c) Find the equilibrium minority-carrier concentrations in each material at 300 K. Assume full ionization of impurities.
d) Find the Fermi level referred to the valence band edge E_V in each material at 300 K. Find also the Fermi level if both types of impurities are present in a single sample (compensation doping

3. From fig. 13 on page 26 of Sze (below), determine what donor atoms are used to dope the Si sample.

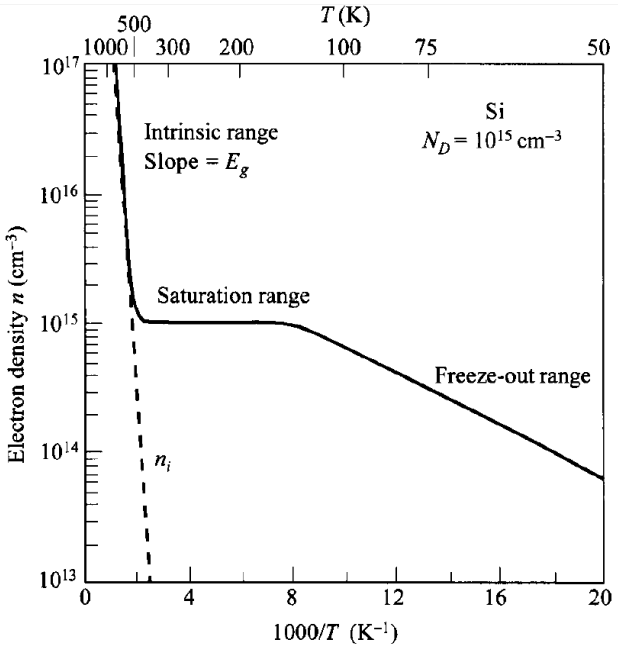


Fig. 13 Electron density as a function of temperature for a Si sample with donor impurity concentration of 10^{15} cm^{-3}. (After Ref. 5.)

4. Consider the Fermi level for a boron-doped Si sample with an impurity concentration of 10^{16} cm^{-3} at 300 K. What fraction of the impurity atoms are ionized? Could we just say that all of them are ionized?
   Hint: select a value for the concentration of ionized acceptors, which also gives you the concentration of holes. Use this to calculate a Fermi level. Use this to evaluate the percentage of ionized acceptors from the Fermi distribution, which you can use to evaluate the Fermi level again. If necessary, repeat until consistent. You can stop after a few iterations….

5. Consider a compensated (contains both donor and acceptor impurity atoms in the same region) n-type Si sample at $T = 300$ K, with a conductivity of $\sigma = 16\ (\Omega\ \text{cm})^{-1}$ and an acceptor doping concentration of 10^{17} cm^{-3}. Determine the donor concentration. Assume complete ionization and an electron mobility of $\mu_n = 1500$ cm^2/Vs. $n_i = 9.65\times10^9$ cm^{-3}.

6. **HAND-IN**

a) Find the resistivity at 300 K for a Si sample doped with 1.0×10^{14} cm^{-3} of phosphorous atoms, 8.5×10^{12} cm^{-3} of arsenic atoms and $1.12\times10^{13}cm^{-3}$ of boron atoms. Assume that the impurities are completely ionized and the mobilities are $\mu_n = 1500$ cm^2/Vs, $\mu_p = 500$ cm^2/Vs, independent of impurity concentrations. $n_i = 9.65\times10^9$ cm^{-3} in Si at 300 K.

b) Find the Fermi level in the sample.

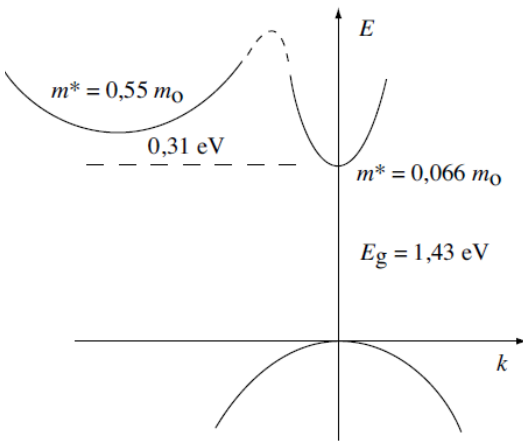
7. Calculate the electron and hole concentration under steady-state illumination in n-type silicon with excess generation rate $G_L = 10^{16}$ $cm^{-3}s^{-1}$, $N_D = 10^{15}$ cm^{-3} and $\tau_n = \tau_p = 10$ μs.

8. **HAND-IN** Assume that an n-type semiconductor is uniformly illuminated, producing a uniform excess generation rate G. Show that in steady state the change in semiconductor conductivity is given by $\Delta\sigma = q(\mu_n + \mu_p)\,\tau_p\,G$.

9. In a Haynes-Shockley experiment, the maximum (excess) amplitudes of the minority carriers at $t_1 = 25$ μs and $t_2 = 100$ μs differ by a factor of 10. Find the minority carrier lifetime.

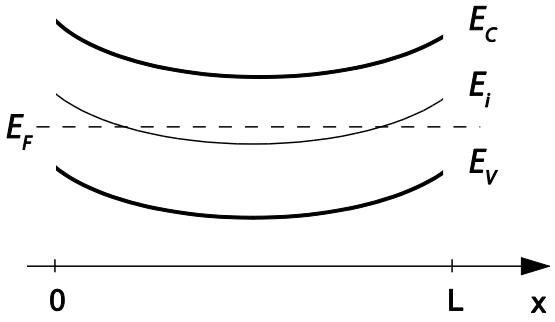
10. The band structure of GaAs is shown to the right. There is a central conduction band minima at the Γ-point and also secondary minima at the L-points, with effective masses as indicated in the figure.

    At high electric fields in n-type GaAs, electrons may be excited from the lower to the higher valley. How is the sample conductivity changed?



11. In an experiment the voltage across a uniform, 2 μm long region of 1 Ωcm, n-type silicon is doubled, but the current only increases by 50%. Explain.

12. The energy band diagram for a semiconductor is shown in the figure to the right. This may for instance represent the variation of potential along the radius of a n-type semiconductor nanowire with the Fermi level pinned close to the valence band edge at the nanowire surface by surface states.

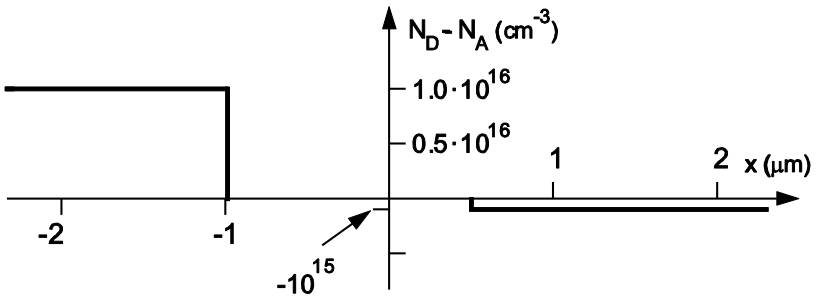


Sketch the general form of

a) n and p versus x,
b) the electrostatic potential V as a function of x,
c) the electric field as a function of x,
d) J_n and J_p versus x.

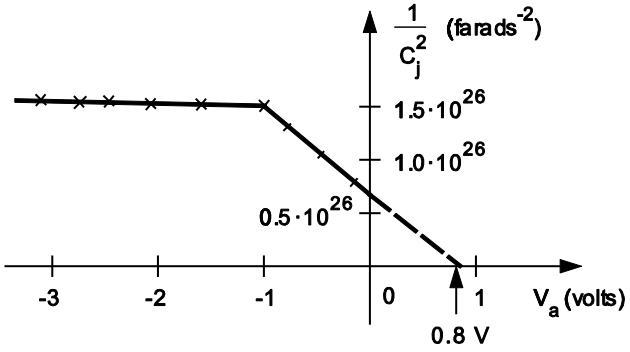
13. Consider an ideal silicon pn abrupt junction with $N_A = 10^{17}$ cm^{-3} and $N_D = 10^{15}$ cm^{-3}. Assume that all impurities are completely ionized.

a) One way of finding an expression for built-in voltage/potential is to consider the p- and n-part of the junction separately. V_{bi} can then be found as the difference between the Fermi-level E_{Fn} on the n-side and the Fermi level E_{Fp} on the p-side, as $qV_{bi} = E_{Fn} - E_{Fp}$. Convince yourself that this gives an equation corresponding to equation 6 on page 81 in Sze.
b) Calculate V_{bi} (Ψ_{bi}) at $T = 300$, 350, 400, 450 and 500 K and plot V_{bi} vs T.
c) Try to give a physical explanation for the trend observed in b). Hint: Maybe you can base your reasoning on the procedure in part a).
d) Find the depletion layer width and the maximum field at zero bias for $T = 300$ K.



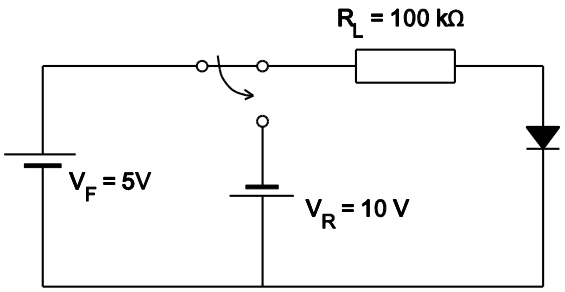
14. **HAND-IN**

a) Find and sketch the charge density, the built-in electric field and the potential for a silicon pin junction with the doping profile shown in the figure above. (The symbol i represents a very lightly doped or nearly intrinsic region.) *See hint on course webpage*
b) Calculate V_{bi} and the length of each depletion region and thermal equilibrium.
c) Compare the maximum field in the pin junction to the maximum field in a pn junction that contains no lightly doped intermediate region, but has the same dopant concentrations as in part (a) in the other regions.
d) Make a sketch indicating how the built-in electrical field in the junction changes when a reverse bias is applied.



15. **HAND-IN** The depletion layer capacitance C_D (denoted C_j in the plot above) of a pn junction diode with area 10^{-5} cm^2 is measured. A plot of $(1/C_D^2)$ vs. the applied voltage V_a is shown in the figure above.

a) If the diode is considered as a one-sided step junction, where the p-side is heavily doped, find the doping level on the n-side.
b) Sketch (qualitatively) the doping density on the n-side of the p^+n junction. Calculate the location of the point (distance from the actual junction) on the n-side at which the dopant density changes, and include this point in your sketch. Indicate how the dopant density changes at this point – does it increase or decrease compared to the value you found in a)?



16. **HAND-IN** In a p^+n silicon diode with $N_D = 10^{15}$ cm^{-3} and $N_A = 10^{18}$ cm^{-3} the lifetime of the holes is 1 μs and their mobility 450 cm^2/Vs. The area of the diode is 0.1 mm^2. ("Ideal" implies that effects within the space-charge region are negligible and that minority carriers flow only by diffusion mechanisms in the charge neutral regions.)

a) Determine the current in the diode when reverse biased as above.
b) Estimate the stored minority carrier charge when the diode is forward biased in the circuit above.
c) Turning the switch will reverse bias the diode. Determine the change in fix charge in the depletion region on the n side when the diode is switched from forward to reverse bias.

17. Consider an ideal, long-base, silicon abrupt pn-junction diode with uniform cross section and constant doping on either side of the junction. The diode is made from 1 Ω-cm p-type and 0,2 Ω - cm n-type materials in which the minority-carrier lifetimes are $\tau_n = 10^{-6}$ s and $\tau_p = 10^{-8}$ s, respectively. ("Ideal" implies that effects within the space-charge region are negligible and that minority carriers flow only by diffusion mechanisms in the charge neutral regions). I used $N_A = 10^{16}$ cm^{-3} and $N_D = 3 \times 10^{16}$ cm^{-3} (from fig 18 on page 32, and I approximated the N_A a little) and I used $D_n = 30$ cm^2/s and $D_p = 10$ cm^2/s when I needed it.

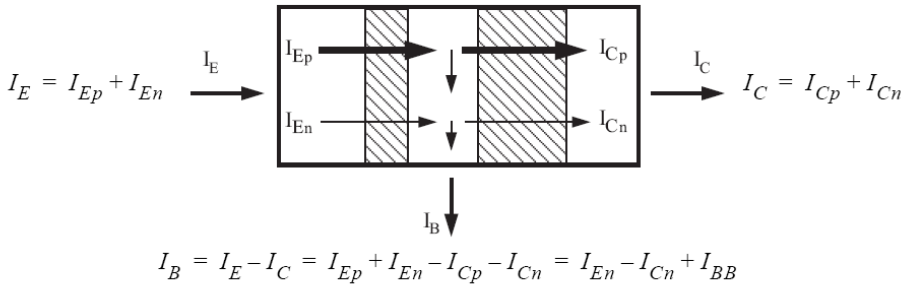
a) What is the value of the built-in voltage (built-in potential)?
b) Calculate the density of the minority carriers at the edge of the space-charge region when the applied voltage is 0,589 V (which is $23 \cdot kT/q$).
c) Sketch the majority- and minority-carrier currents as functions of distance from the junction on both sides of the junction, under the applied bias voltage of part b.
d) Calculate the location(s) of the plane or planes at which the minority-carrier and majority-carrier currents are equal in magnitude for the applied bias of part b.

18. For forward voltages between 0 and 0.75 V, plot (on a logarithmic scale) the diffusion current in a Si p^+n-junction. In the same plot, include also the recombination current (eq 74 on page 98). You may assume a donor concentrations of $N_D = 10^{15}$ cm^{-3}, $\mu_p = 500$ cm^2/Vs and $D_p = 10$ cm^2/s and a life-time $\tau_p = \tau = 1$ μs. For the purpose of calculating the built-in potential you can use for instance $N_A = 10^{17}$ cm^{-3}.

Finally, plot the sum of the two current contributions, also in the same plot. Try to identify regions with ideality factor 1 or 2 (see eq. 78 on page 98 for definition of ideality factor)

19. A Si *npn* transistor has impurity concentrations of 5×10^{18}, 2×10^{17} and 10^{16} cm^{-3} in the emitter, base and collector, respectively. The p-type base width is 1.0 μm, and the device cross-sectional area is 0.2 mm^2. When the emitter-base junction is forward biased to 0.5 V and the base-collector junction is reverse biased to 5 V, calculate

a) the neutral base width and
b) the minority carrier concentration in the base at the edge of the emitter-base junction depletion region.



20. **HAND-IN** The figure above depicts a *pnp* bipolar transistor and all the currents which we consider in it.

a) Draw an equivalent figure, still for a *pnp*-transistor, where you instead of currents draw *electron and hole flows.*
b) Draw an equivalent figure for a *npn* transistor, where you draw *currents.* Label the currents in a way appropriate to the npn-transistor.

Make nice big figures, so that everything is clearly visible.

21. **HAND-IN**

Consider equations 2-4 on page 246-247 in Sze for the distribution of minority carriers in the base of an *npn* bipolar transistor in the active mode (EB junction forward biased and BC junction reverse biased). The equations can be reorganized to read:

$$n_p(x) - n_{p0} = \left(n_p(0) - n_{p0}\right)\frac{\sinh\left(\frac{W-x}{L_n}\right)}{\sinh\left(\frac{W}{L_n}\right)} + \left(n_p(W) - n_{p0}\right)\frac{\sinh\left(\frac{x}{L_n}\right)}{\sinh\left(\frac{W}{L_n}\right)}$$

where $x = 0$ and $x = W$ are the edges of the neutral base (as in fig 3b on page 246 in Sze). This equation is similar to that of page 61 in the handout, only there we consider minority carriers (holes) in the n-type base of a pnp-transistor.

a) For a Si npn-transistor, plot $n_p(x)/n_{p0}$ as a function of x/W for different values of W. In your plot, include the following neutral base widths W:

W/L_n = 100, 10, 5, 2, 1, 0.5, 0.1 and 0.01.

All graphs should be in the same plot (this is why the x-axis should be normalized to x/W). You can assume V_{EB} = 0.5 V, V_{CB} = -1 V, $N_B = 1 \cdot 10^{16}$ cm^{-3} and $L_n = 1 \cdot 10^{-4}$ cm (the minority carrier diffusion length in the base).

b) Using the plots in a), evaluate the ratio I_{Cn}/I_{En} for the different base widths W. *Hint – the currents can be obtained by estimating the gradients of the minority carrier distributions.*

Make a graph where you plot the ratios I_{Cn}/I_{En} for different W vs W. Since W varies over four orders of magnitude, you need to use a logarithmic scale on the x-axis. Verify your results by comparing your ratios to the theoretical ratio $\frac{I_{Cn}}{I_{En}} = \frac{1}{\cosh(W/L_n)}$.

c) Write a short text (~ 100-150 words is sufficient) describing how your plots are significant to our discussion of bipolar transistors.

22. **HAND-IN** Consider a Si *npn* transistor. The area of the device is $1.2 \cdot 10^{-4}$ cm^2. In absence of applied bias, the neutral base width is $4 \cdot 10^{-4}$ cm. For the transistor we further have:

$N_E = 3.9 \cdot 10^{17}$ cm^{-3}	$N_{EB} = 1.6 \cdot 10^{16}$ cm^{-3}	$N_{EC} = 2 \cdot 10^{14}$ cm^{-3}
$L_E = 22.8 \cdot 10^{-4}$ cm	$L_B = 46.9 \cdot 10^{-4}$ cm	$L_C = 39.5 \cdot 10^{-4}$ cm
$D_E = 5.18$ cm^2/s	$D_B = 22$ cm^2/s	$D_C = 15.6$ cm^2/s

a) Calculate I_{En} and I_{Ep} (it is OK to use the expressions for current for short bases, that is, when $W/L_n < 1$). Also calculate the emitter efficiency γ for a forward bias of V_{EB} = 0.6 V on the emitter-base junction. You don't need to case about the change in W due to biasing.

b) What is the emitter efficiency if the emitter is doped to the same level as the base, that is, $N_E = N_B = 1.6 \cdot 10^{16}$ cm^{-3}?

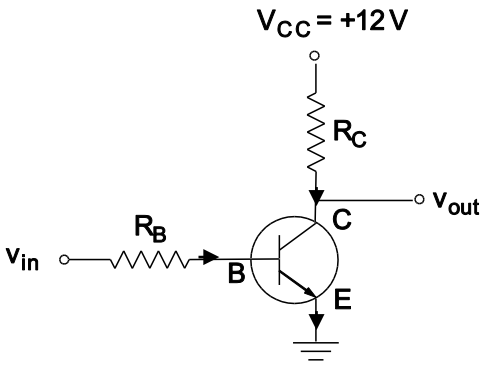
23. For the transistor of problem ~~21~~22, consider the emitter-base junction open-circuited and the base-collector junction reverse biased by -1 V. Find V_{EB} and I_{CBO} (that is the current in the base-collector junction when the emitter current is zero). The neutral base width in the absence of applied biases is stated in problem 22. Here, there is a reverse bias applied to the base-collector junction. Since the collector is lightly doped the depletion region at the base-collector junction will expand mainly into the collector, and thus the base width will not be significantly reduced. You can use the value of problem 22 as the base width W.

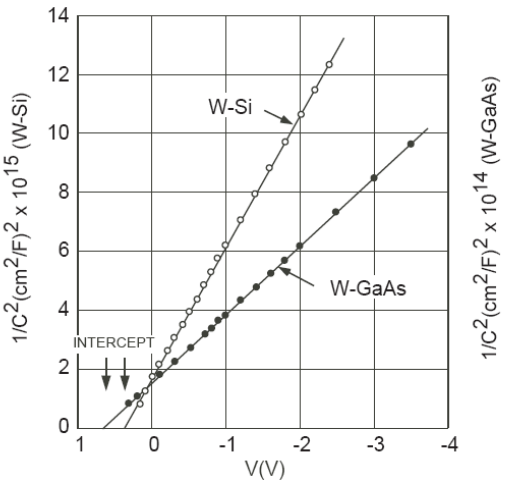
24. Consider the lower image on p 64 of the notes. It shows band diagrams for a pnp-transistor in the four modes of operation. Draw the equivalent images for a npn transistor.

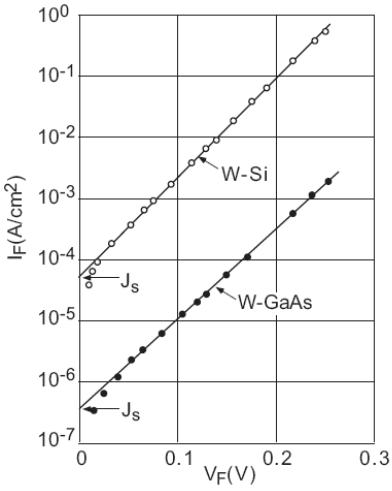
25. The transistor in the circuit shown in the figure has a common-emitter current gain β = 100. The resistors in the circuit are R_C = 1 kΩ and R_B = 20 kΩ.

Determine v_{out} for v_{in} = 1 V and 2 V.

Assume V_{EB} = 0.6 V for the forward biased EB junction.







26.**HAND-IN**

a) Find the barrier height and the donor concentration of the W- GaAs Schottky barrier shown in the capacitance plot above left. We ignore the "image-force lowering" $\Delta\phi$.

b) Compare the barrier height with that obtained from the saturation current density shown in the current plot above right, assuming that A**= 4 A/(cm-K)^2. (Equation 111 is a more elaborate version of what we have on page 79 in the handouts – we again ignored $\Delta\phi$. A** is the reduced Richardson factor which involves effects of tunneling, but which differs less than an order of magnitude from A**, so you can use A*=A** here.)

27. Compare a Schottky diode fabricated on n-GaAs and a p$^+$n diode (also GaAs). The reverse saturation currents are $I_s = 5\times10^{-9}$ A and $I_0 = 10^{-13}$ A for the Schottky diode and the pn-junction, respectively. What voltage is required for each device in order to have 0.5 mA pass through it?

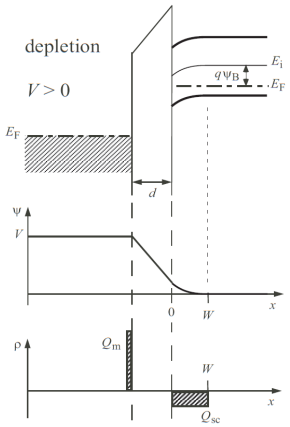
28. a) In figure 6 on page 143 we notice that $c_2 = 0.27$ is relevant for Si. This number thus tells us something about the nature of the population of surface states in Si. Assuming an interface layer with thickness $\delta = 5$ Å and permittivity $\varepsilon_i = \varepsilon_0$ and a semiconductor doping of $N_D = 10^{18}$ cm^{-3}, calculate the density of interface states D_{it}. (check your answer on page 142).

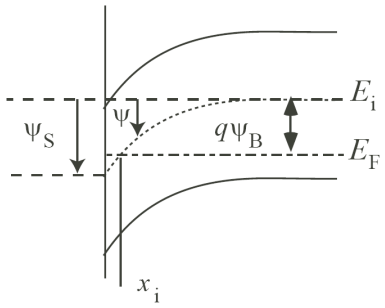
b) If the Fermi level does not coincide with the neutral level, there will be a net charge at the interface. By how much can the Fermi level deviate from the neutral level in order for the interface charge Q_{ss} to not become greater than the semiconductor charge Q_{sc} (from ionized dopants)? Here you will have to obtain a value for V_{bi} (Ψ_{bi}) at some point. Either you can just assume some reasonable value, or use fig. 5 on page 140 in the book. $\Psi_{bi} = E_g - q\phi_n - q\phi_0$, if we make the approximation that E_F coincides with $q\phi_0$ (not completely true, but not far from the truth either, it will do as an estimate). $q\phi_0$ is calculated at the bottom of p. 142.

29. For an ideal n-type semiconductor under inversion, plot

a) the charge distribution
b) the electric field
c) the potential

30.





We want to find the threshold voltage V_T for inversion in a p-type Si MOS in terms of material constants, such as dielectric constants, and in terms of parameters that we control, such as doping level. The voltage drop V_T is split between the oxide and the semiconductor, so that $V_T = \Psi_S + V_o$.

The band bending (in inversion) is primarily given by the depleted region in the semiconductor. Here, we have a space charge density $\rho = -qN_A$ for $0 \le x \le W$ (see figure). From that we find the potential

$$\Psi(x) = \frac{qN_A}{2\varepsilon_S}(x - W)^2 = \Psi_s(1 - \frac{x}{W})^2,$$

where $\Psi_s = \frac{qN_A}{2\varepsilon_S}W^2$ is the potential on the semiconductor surface.

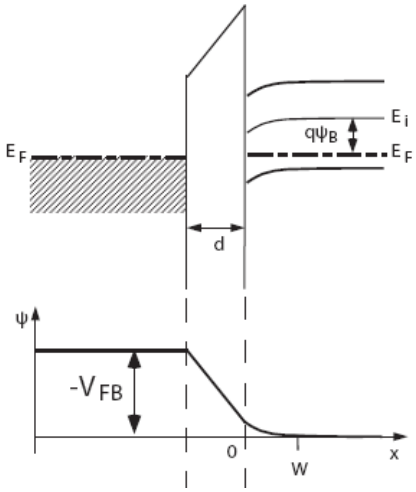
a) Deep in the p-type semiconductor $p_{p0} = N_A$.
Starting from $p = n_i e^{(E_i - E_F)/kT}$ show that $\Psi_B = \frac{kT}{q}\ln\frac{N_A}{n_i}$.

b) In strong inversion the electron concentration at the surface $n_s \ge N_A$.
Starting from $n_s = n_i e^{(E_F - E_{is})/kT}$, where E_{is} is the intrinsic Fermi level at the surface, show that $E_F - E_{is} = \Psi_B$ when $n_s = N_A$. The potential at the surface thus has to be $\Psi_S = 2\Psi_B$ for inversion.

c) Now consider the voltage drop V_o over the oxide. From electrostatics, we found that $V_o = d\frac{Q_m}{\varepsilon_{ox}} = d\frac{|Q_S|}{\varepsilon_{ox}}$. At the onset of strong inversion, $|Q_s|$ can be approximated by $|Q_{sc}|$ where Q_{sc} is the charge from the depleted acceptors. In inversion, $Q_{sc} = -qN_A W_m$.

Show that the depletion region width W can be written in terms of the surface potential as $W = \sqrt{\frac{2\varepsilon_S \Psi_S}{qN_A}}$ (see beginning of problem) and that, consequently, in inversion, $W_m = \sqrt{\frac{2\varepsilon_S 2\Psi_B}{qN_A}}$.

d) Now we put our results together.
Show that the threshold voltage $V_T = \Psi_S(\text{inv}) + V_o = \frac{2kT}{q}\ln\frac{N_A}{n_i} + \sqrt{\frac{4\varepsilon_S N_A d^2}{\varepsilon_{ox}^2}kT\ln\frac{N_A}{n_i}}$



31. **HAND-IN** For the MOS structure above, the work function in the metal is smaller than that of the semiconductor by 1V (we disregard any oxide charges). The potential difference $|V_{FB}|$ between metal and semiconductor is composed of a potential drop over the oxide and a potential drop over the depleted region of the semiconductor. Consider the semiconductor to be grounded. The oxide thickness d =10 nm, the oxide permittivity is $\varepsilon_{ox} = 3.9\varepsilon_0$ and $N_A = 10^{17}$ cm^{-3}.

a) What is the value of the surface potential?
b) What is the electric field in the oxide?
c) What are the values of electron and hole concentrations at the surface of the semiconductor?

32. Consider a MOS device on a p-type substrate (N_A=10^{17} cm^{-3}) with 20 nm of gate oxide. The gate is made of polycrystalline n$^+$-Si. When used as a gate electrode, the n$^+$-Si is very heavily doped and essentially the Fermi level coincides with the conduction band edge.

a) Find the work function difference between the polycrystalline Si gate and the p-type Si semiconductor.
b) Find V_T.
c) Make a sketch of the C-V curve measured at high frequencies. In your sketch, label (roughly) V_T and V_{FB}.
d) Calculate C_{min} and and C_{max} (still for high frequency). The e-book differentiates between C_{min} and C'_{min} – let's think of C_{min} as the value of C at V_T.

33. Threshold voltage control is an important concept. In devices such as CMOS (Complimentary MOS – one PMOS and one NMOS acting together as for instance an inverter) and generally in circuits, we may want to tailor the threshold voltage. There are several approaches to this.

Consider a N-MOS with gate and semiconductor parameters as in problem 32.

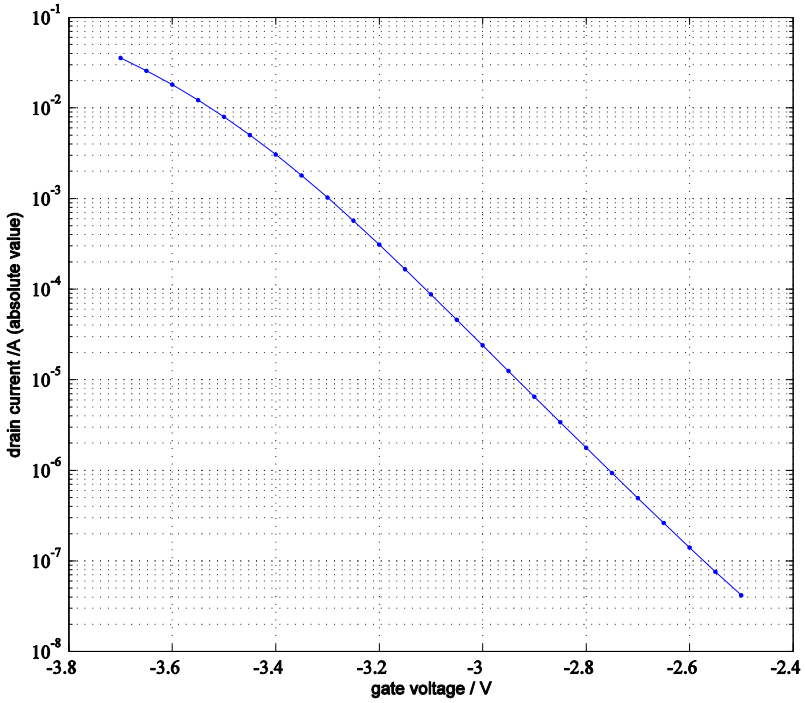
a) Is the N-MOS conducting at $V_G = 0$?
b) Find the change in doping necessary to change V_T by -0.5 V. Here, we assume that the doping is changed to a large depth in the semiconductor, not only just below the oxide.
c) Find the change in oxide thickness needed to accomplish the same shift of V_T as in b)

34. A n-channel MOSFET is made on p-type silicon with $N_A = 4\times10^{15}$ cm^{-3}.
a) Determine the threshold voltage under the assumption that the oxide (rel. dielectric constant 3.9) is free of charge and that difference in work functions may be neglected. The gate oxide is 100 nm thick.
b) Sketch the drain current vs the gate voltage for the MOSFET of part a) if drain and gate are connected and source and substrate are grounded. Can the threshold voltage be determined from the characteristic?

35 **HAND-IN**

a) A MOSFET has a threshold voltage of V_T = 0.5 V, a subthreshold swing of 100 mV/decade, and a drain current of 0.1 mA at V_T. What is the subthreshold leakage current at V_G = 0V? (*Hint: think about what the subthreshold swing really means.*)

b) In the MOSFET lab, you measured drain current as a function of gate and drain voltage. The figure shows the drain current at a fixed $V_D > V_{Dsat}$) for varying V_G for one of the devices in the lab. Was it the NMOS or the PMOS and what is the subthreshold swing?



36. Consider an n-channel Si MOSFET with 20 nm thick gate oxide (relative dielectric constant 3.9) and uniform p-type substrate doping of 10^{17} cm^{-3}. The dimensions are $Z = L$ =1 μm and the electron mobility in the inversion layer is 800 cm^2/Vs. The semiconductor work function is 3.8 V and the gate work function is 4 V.

a) Sketch the band diagram at thermal equilibrium. Sketch the band diagram at threshold condition $\Psi_s = 2\Psi_B$. What is the threshold voltage?

b) Calculate the drain current for V_G = +2.2 V and V_D = 0.4 V.

c) What length can the channel be reduced to before severe short-channel effects take place? (See handout on short-channel MOSFETs).