Laboratory exercise: The MOS-Transistor

Semiconductor Physics 2016

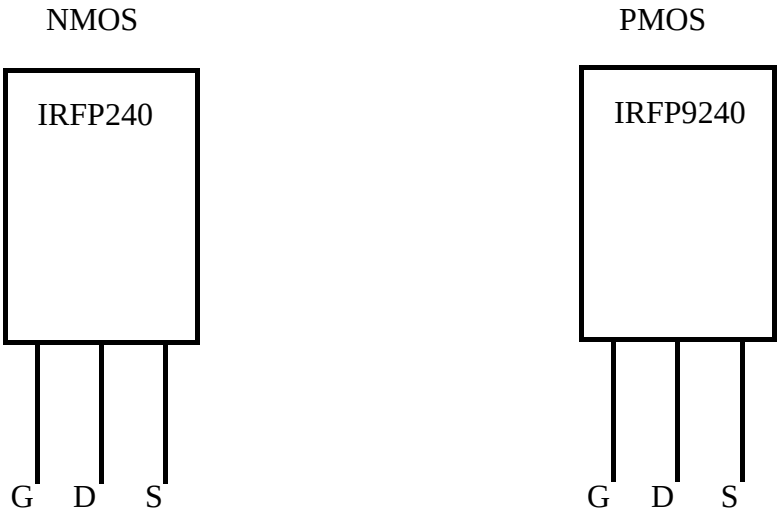
Lab meeting point – k-space at Solid State Physics

This second laboratory exercise consists of two experimental parts and one simulation part. We will investigate Si MOS-transistors and study their current-voltage characteristics and the internal band bending as a function of applied biases. Thereby we hope to elucidate the intrinsic physical processes in the device structures.

In the first experimental part you will be measuring IV-characteristics as a set of IV-curves. In the second experimental part you will modify the "fan circuit" from the BJT-lab in order to make it work with a MOSFET. In the simulation part you will use the same simulation tool as in the previous lab in order to study the physical parameters of the device.
As a preparation for this exercise we recommend that you study the chapter about MOS-transistors in the text book and the handouts. Also take a look at the schematics you made for the "fan circuit" in the previous lab

Experimental Part One:

In this part of the exercise we will be measuring the I_D-V_{DS} characteristics for varying gate voltages. The idea is to deduce fundamental properties like the transconductance and then compare the results for a NMOS- and a PMOS- transistor.



The figure shows a sketch of the NMOS and PMOS transistors you should characterize.

Connect the source to ground and apply the potential on the drain and gate contacts

NMOS: Measure the IV-characteristics using the following parameters

- V_G = 2.5 ... 3.7V in steps of 50 mV
- V_{DS} = 0 ... 2.5V in steps of 10 mV

PMOS: Measure the IV-characteristics using the following parameters

- V_G = -2.5 ... -3.7V in steps of 50 mV
- V_{DS} = 0 ... -2.5V in steps of 10 mV

Data Analysis for the PMOS and NMOS

"Transconductance" is not mentioned in the lecture notes, but is defined on page 187 in Sze (p 191 in 2nd edition).

$$g_m = \frac{dI_D}{dV_G}$$

To make an analogy with bipolar transistors, remember that $I_C = \beta \cdot I_B$, that is, I_C is controlled by I_B with an amplification β. Now, in the MOSFET, we have no amplification but instead a transconductance describing how the drain current is controlled by gate voltage; $dI_D = g_m dV_G$.

a) Calculate the transconductance at a specific point (V_{DS} = 2V, V_G = 3.7V) in the saturated region – how much did the drain current change as the gate voltage was stepped between 3.65 V and 3.7 V?

b) Do the same analysis for all the steps in gate voltage – still for V_{DS} = 2V. Make a plot of transconductance vs. gate voltage.

c) Consider a constant gate voltage of 3.7 V – choose one of the traces in the IV-curves we measured. Calculate the conductance of the inverted channel along this trace in the linear region (before we reach saturation).

$$g_D = \frac{dI_D}{dV_{DS}}$$

which can be found taking the derivative of eq. 36 on page 185 in Sze or page 88 in the notes. For very small V_{DS}, this equation could be simplified further to read $I_D = \frac{Z}{L}\mu_n C_o (V_G - V_T) V_{DS}$ (linear regime).

d) Plot the square root of drain current vs the gate voltage at V_{DS} = 2V. We are now in the saturated regime, where $I_D = \frac{Z\mu_n C_o}{2L}(V_G - V_T)^2$. Taking the square root should give you a straight line, at least at high gate voltages. Estimate the threshold voltages for the NMOS and the PMOS by extrapolating to $I_D = 0$.

e-h) make the same analysis for PMOS by reversing the signs.

Final analysis: Choose gate voltages such that (V_G-V_T) is the same for both devices. Compare

the conductance at these values of gate voltages for the two devices. Assuming that the oxide capacitance is the same, what can you say about Z/L for the two components? Remember that hole and electron mobility differs. Z is the width of the transistor, as seen on page 87 of the notes or on p 182 in Sze (p 186 in 2nd edition) and L is the channel length.

Experimental Part Two:

The base of a BJT consumes some base-current. In the previous laboratory exercise we amplified the small current from a photo resistor to a current large enough to drive a small computer fan. The gate of the MOSFET is completely isolated and thereby consumes no current at all.

- Figure out how to modify the circuit so that it works with a MOSFET.
- Do the necessary calculations and assemble the circuit on the prototype board. Note that the fan needs to be connected in the right way – red to positive pole!
- Test it!
- Measure the voltage over the fan at high and low illumination.
- Measure the voltage at the gate at high and low illumination.

Simulation:

In this simulation we will first study how the potential structure inside the MOSFET changes with applied gate bias. The potential on the source and drain is thus put to zero volt and a bias is applied to the gate.

Next, we apply a bias also to the drain and study the IV- characteristics at a fixed gate bias of -2V. In this simulation sequence we will also deduce the band structure in the device as a function of the drain bias. When comparing these sets of data you will hopefully gain a deeper insight into the physical mechanisms inside the MOSFET.

The device structure is a Si MOSFET which is formed on an n-type substrate. Heavily doped p- type regions are used as source and drain and aluminum is used as the gate electrode.
During this simulation 4 windows will appear in Tonyplot with the data from the calculations. These plots are:

1) Basic structure at zero gate bias and zero drain bias with a vertical cross-section.
2) Basic structure at varying gate bias (+1V, 0V,-2V) with a vertical cross-section
3) I_d vs. V_d at V_g=-2V
4) Basic structure at varying V_d (0V, -1V, -2V) and fixed V_g of -2V with a lateral cross-section.

Start the simulation tool **Silvaco Deckbuild** (shortcut on the desktop). For the license the computer must be connected to the license server via LU Web-logon.

Load **mos.in** located in c:\SilvacoWork\MOSFET\

Run the simulation by clicking on the green arrow.

Simulation/Analysis:

- **Plot one**

a) Analyze the geometry of the device by inspecting the device structure.
b) What is the surface potential at the Si/SiO_2 interface? (right-click in the cross-section plot and then choose conduction band and/or potential)
c) How large is the Flat Band Voltage, V_{FB}?
d) Use the simulated data to calculate the threshold voltage. The oxide thickness is 12 nm. (Hint: Ψ_B can be deduced from the simulated data – check in the book or lecture notes how Ψ_B is defined. How does V_{FB} enter into the threshold voltage?) Also find N_D from Ψ_B.

- **Plot two**

a) What are the values for the surface potential and the voltage drop across the oxide for the various gate voltages?
b) Estimate the surface concentrations of majority and minority carriers for the different voltage conditions. Is the law of mass action valid? Also, check the Fermi

level energy (Electron or hole QFL in Silvaco) relative to the band edges – are these consistent with a non-degenerate semiconductor (which is a prerequisite for the law of mass action to be valid)?

- **Plot three**

a) Remind yourself - which type of carriers do we have (electron or holes) in the channel?
b) Is the simulated IV-curve corresponding to your expectations?
c) What is the polarity of the drain bias? Given that, what is the direction of current (S to D or D to S)?

- **Plot four**

a) Investigate the displayed cross-section of the device for varying drain biases. (This cross-section is already displayed and is taken 14nm below the Si/SiO2 interface.)
b) How is the band structure affected by the drain bias? (look at conduction band energy and valence band energy)
c) What is the maximum electric field? Note that the coordinate system is such that *x* is along the channel and *y* is perpendicular to the channel.
d) Consider electric fields in *x*-direction (along the channel) and in the *y*-direction (perpendicular to the oxide). Can you make sense of the plots? For the long channel devices that we are presently considering, we are assuming that the gate controls the channel and that V_d doesn't significantly changing the channel properties. This means that the electric field in the channel in the y-direction (caused by the gate) should be much stronger than along the channel from V_d. Is that true for all the applied biases in your plot?

For the lab report:

Again, you don't have to write a "full" report. However, your text should clearly show that you have understood the concepts, plots and results. In particular, consider the following:

a) Experimental part one: plot the measured data of the transistors and your deduced plots of transconductance and conductance. Answer the questions in the text.
b) Simulation part: discuss the plots and the results you deduce from them. Answer the questions in the text.
c) Experimental part two: show a sketch of the circuit. Answer the questions in the text.